

FIG. 1

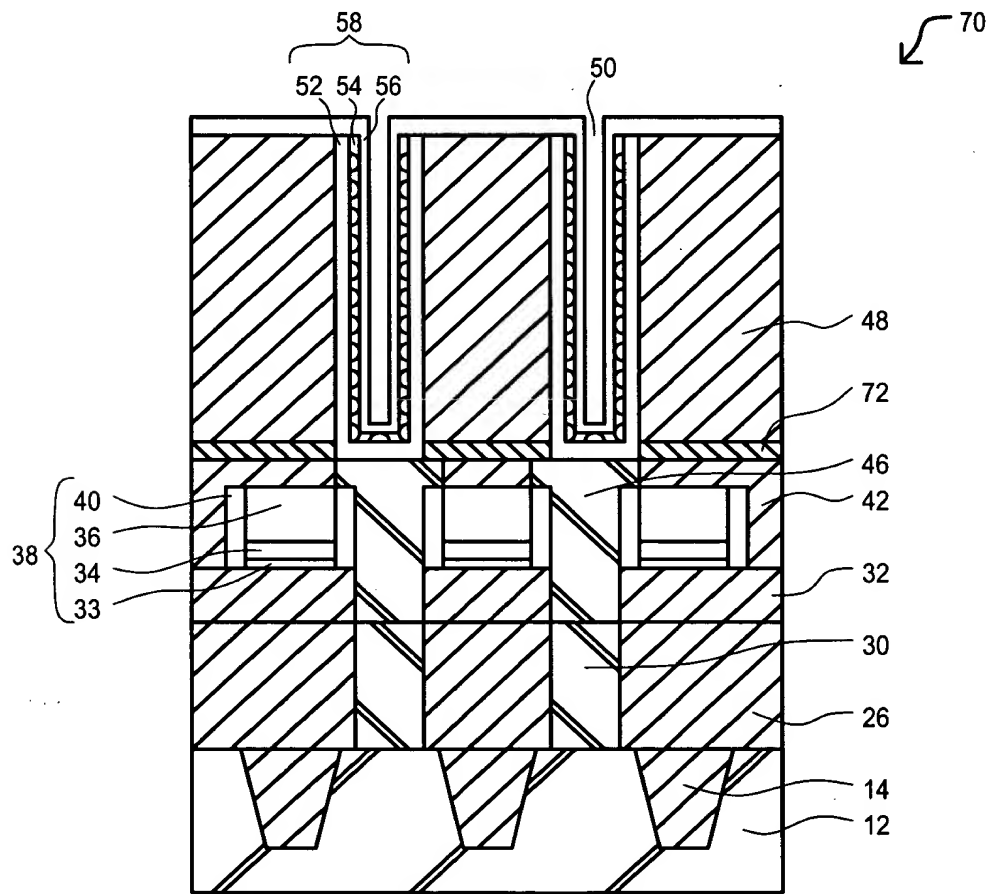
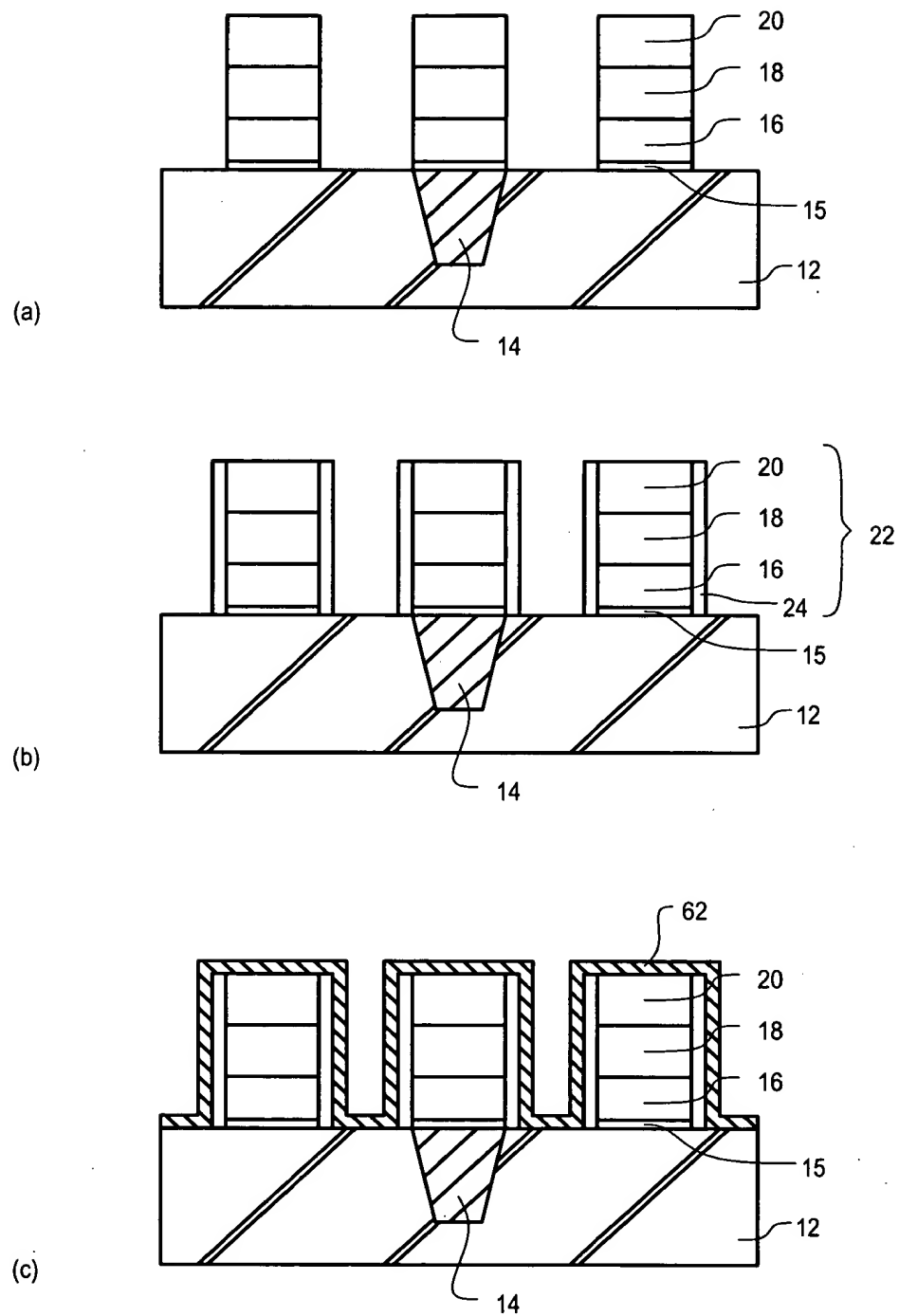


FIG. 4

FIG. 2



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FIG. 3

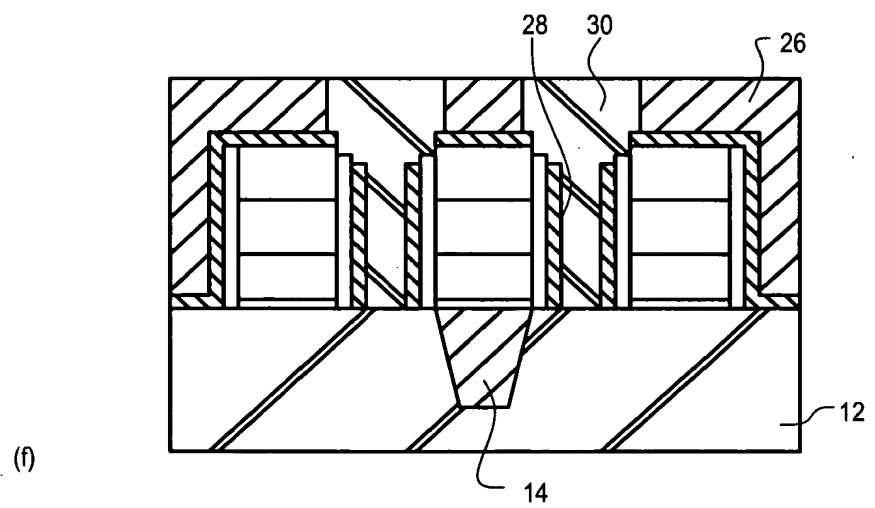
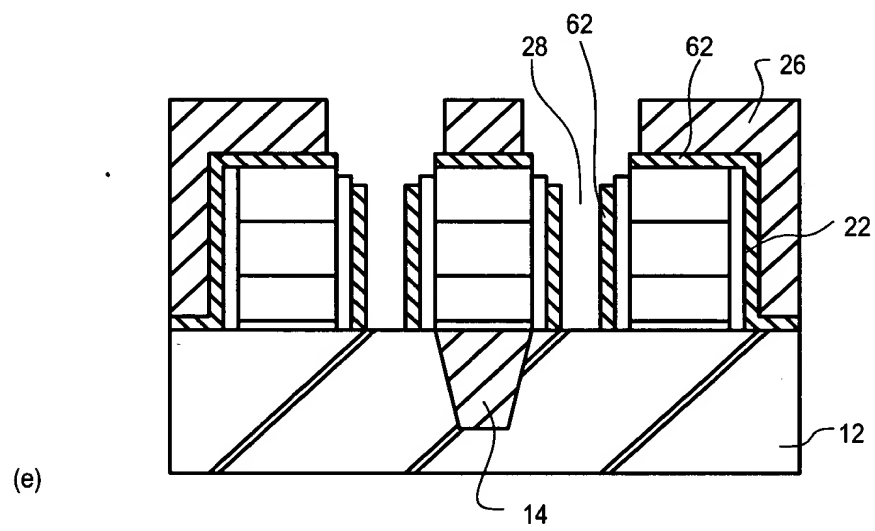
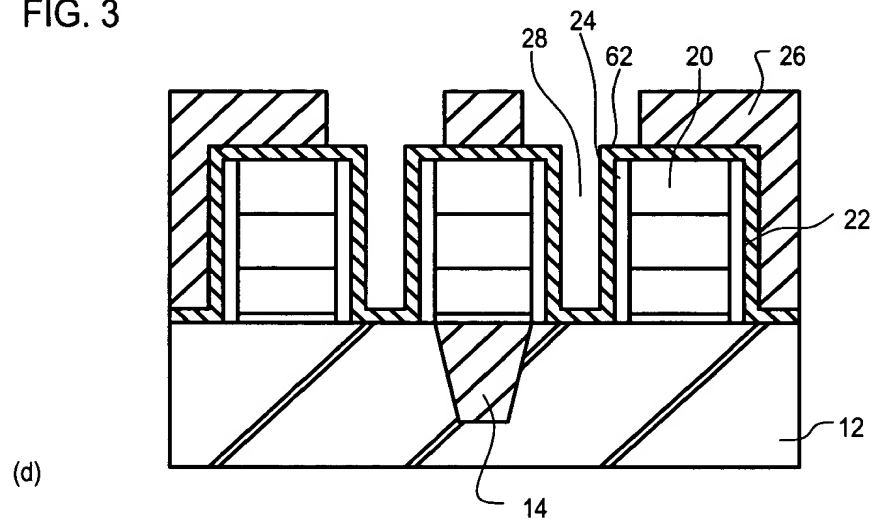


FIG. 5

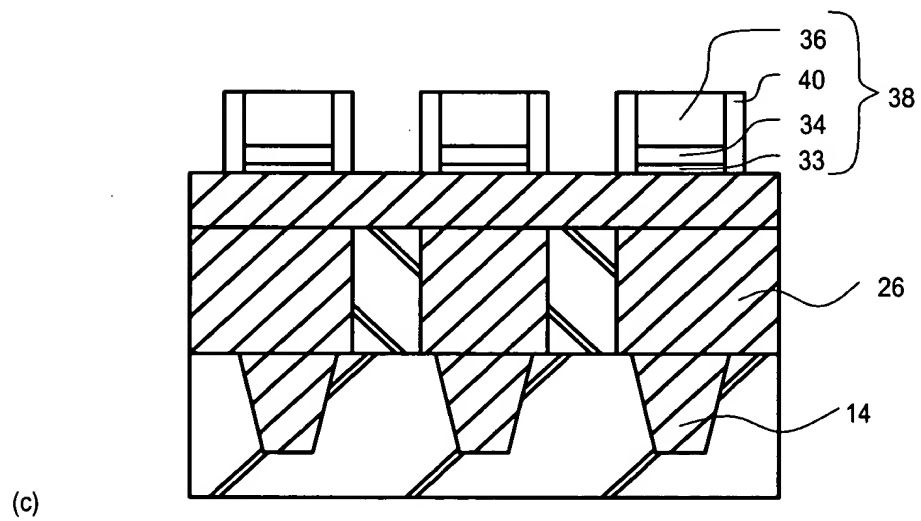
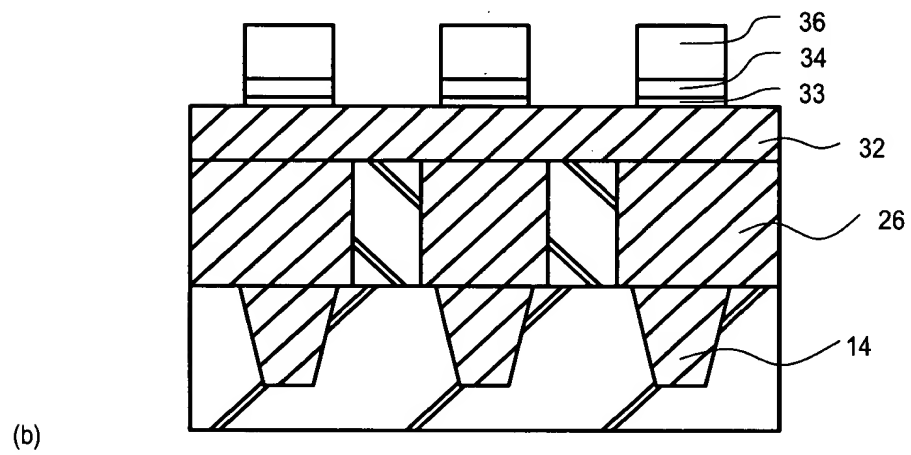
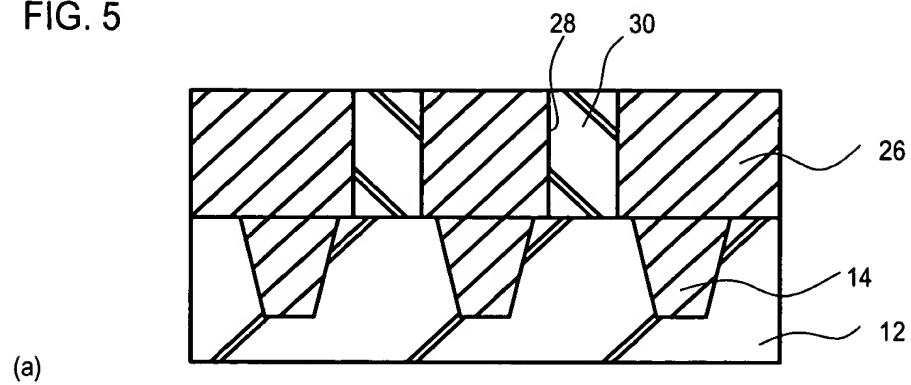


FIG. 6

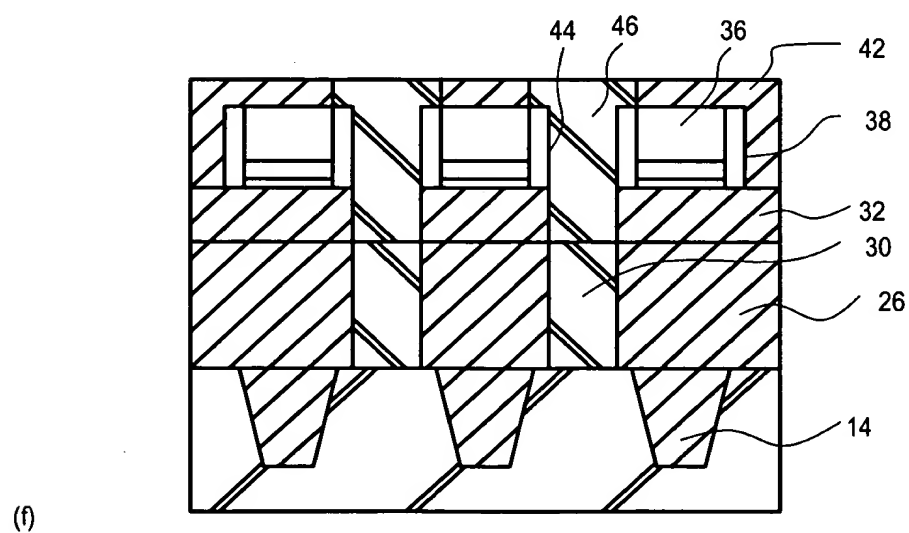
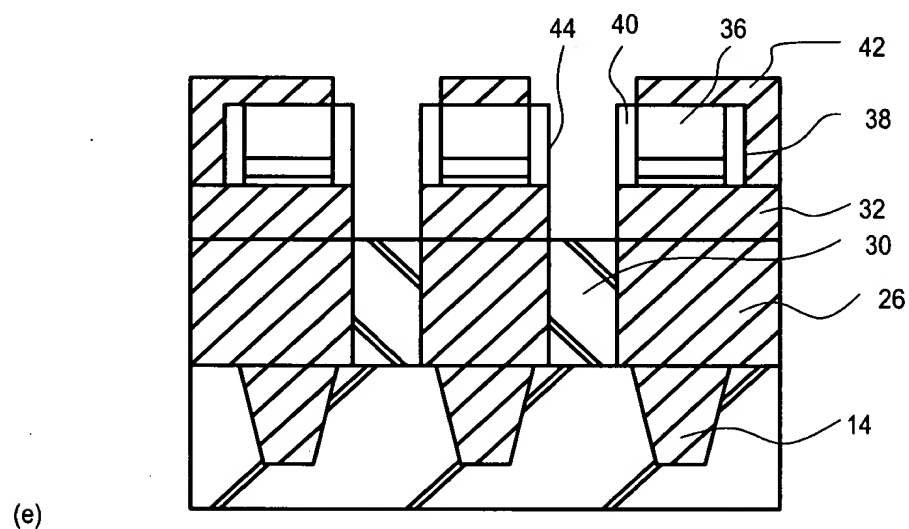
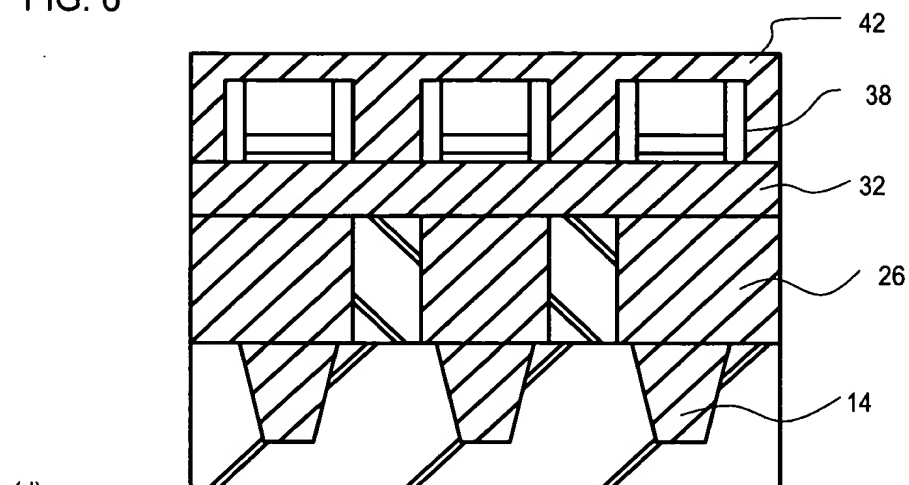
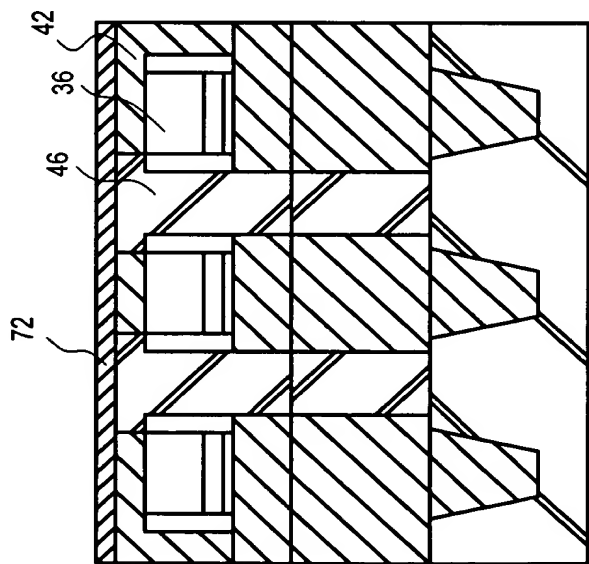
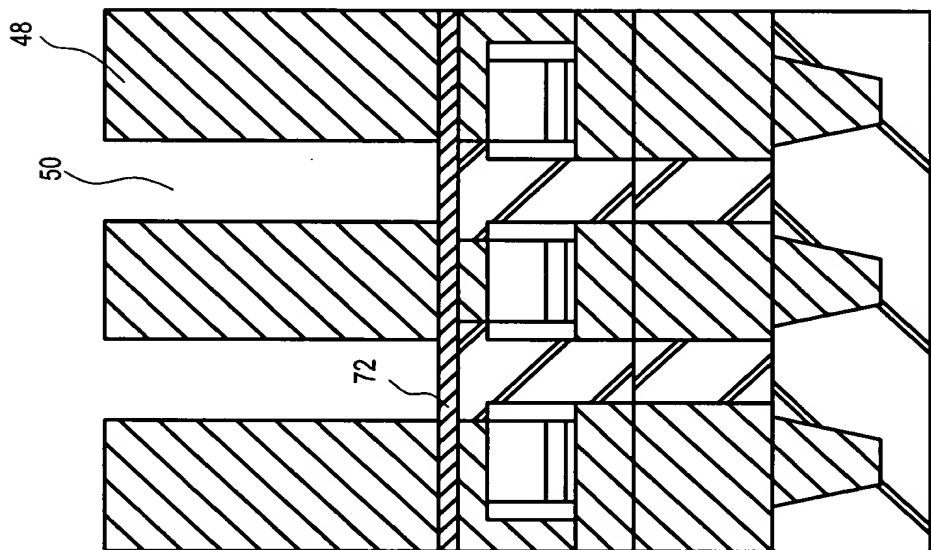


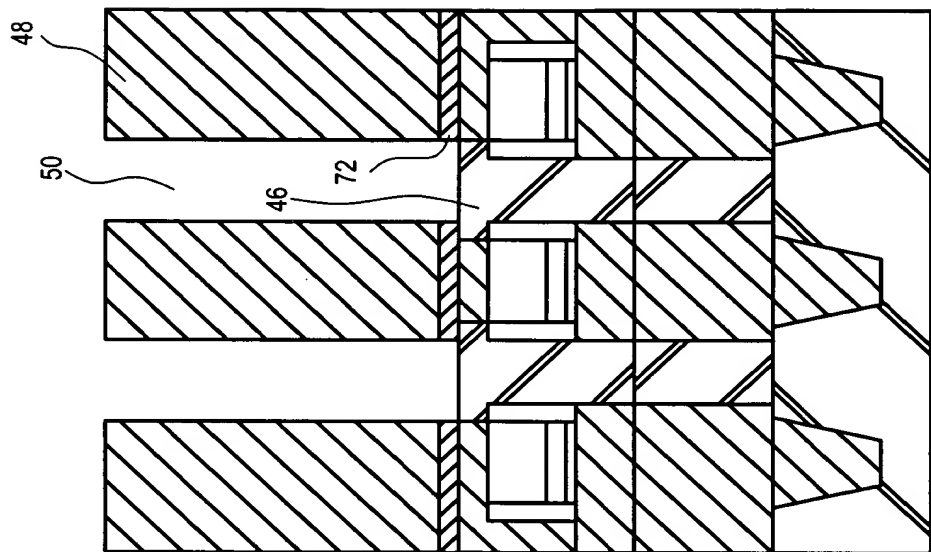
FIG. 7



(g)

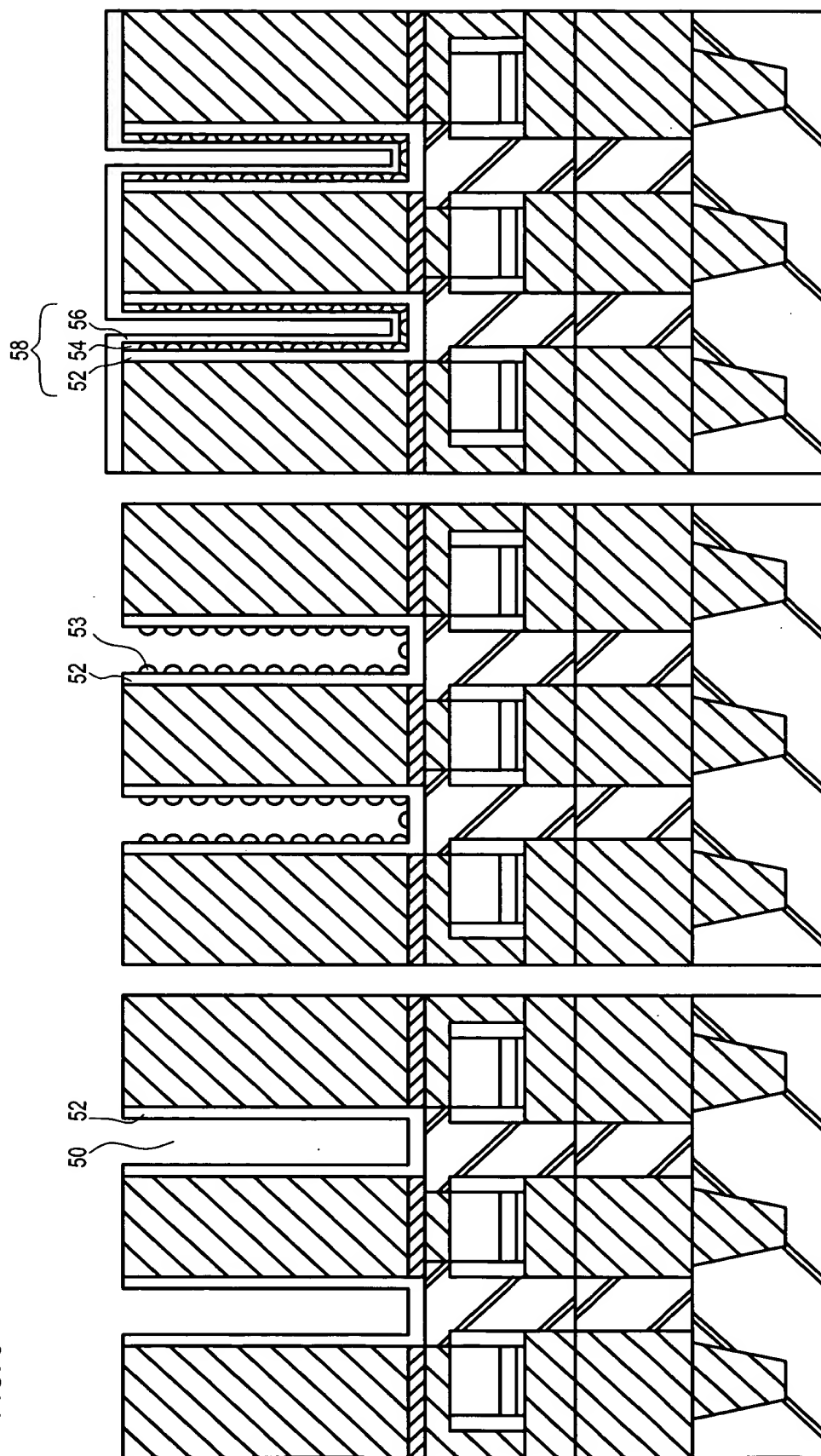


(h)



(i)

FIG. 8

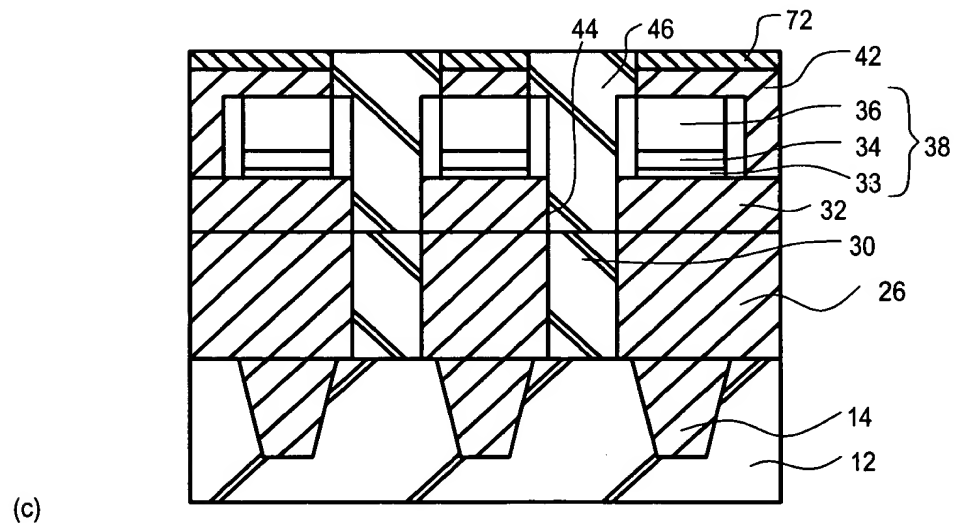
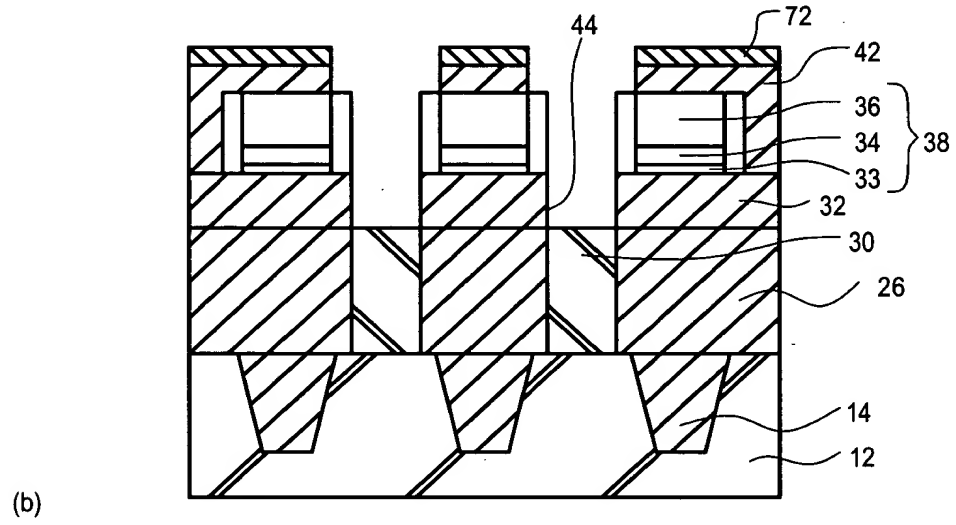
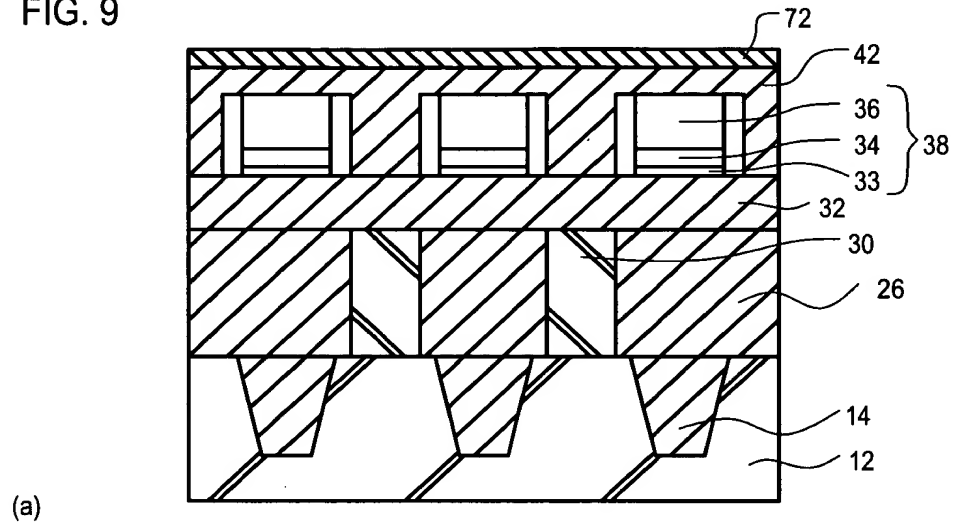


(J)

(K)

(L)

FIG. 9



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FIG. 10

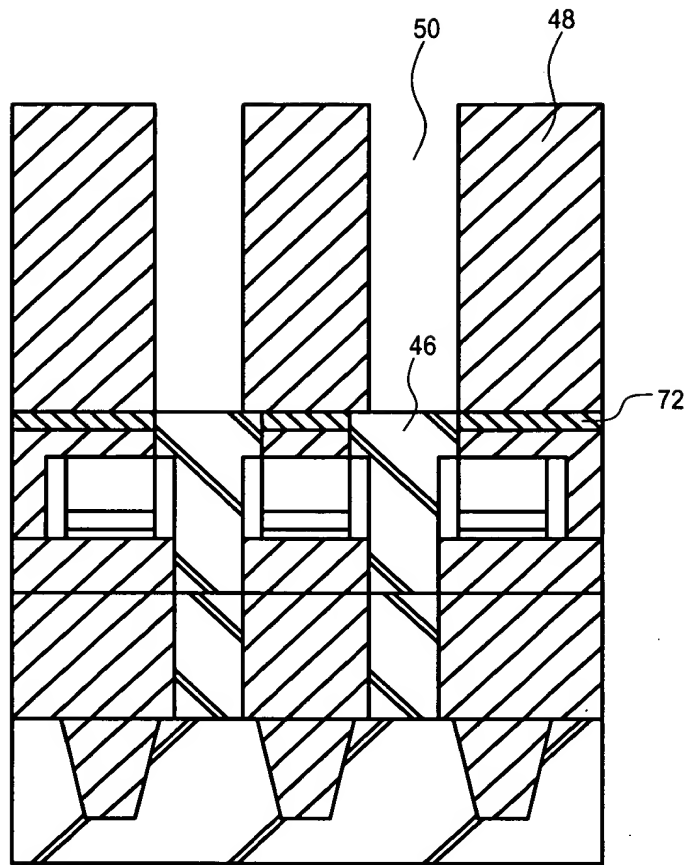


FIG. 11

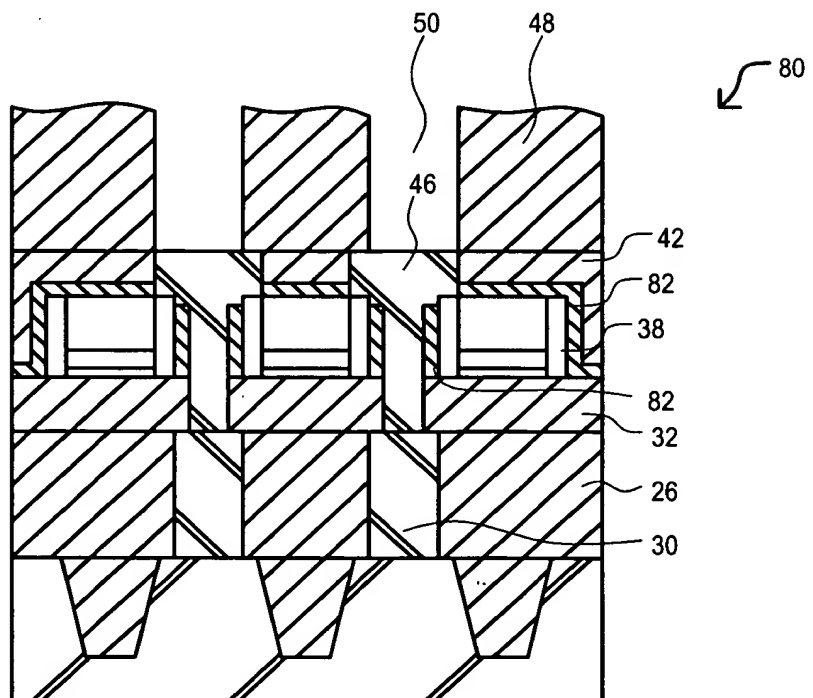
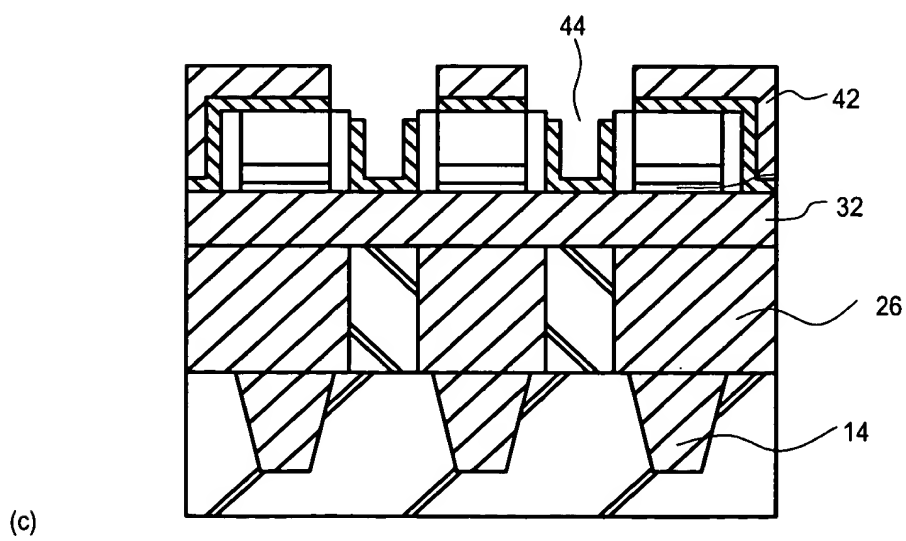
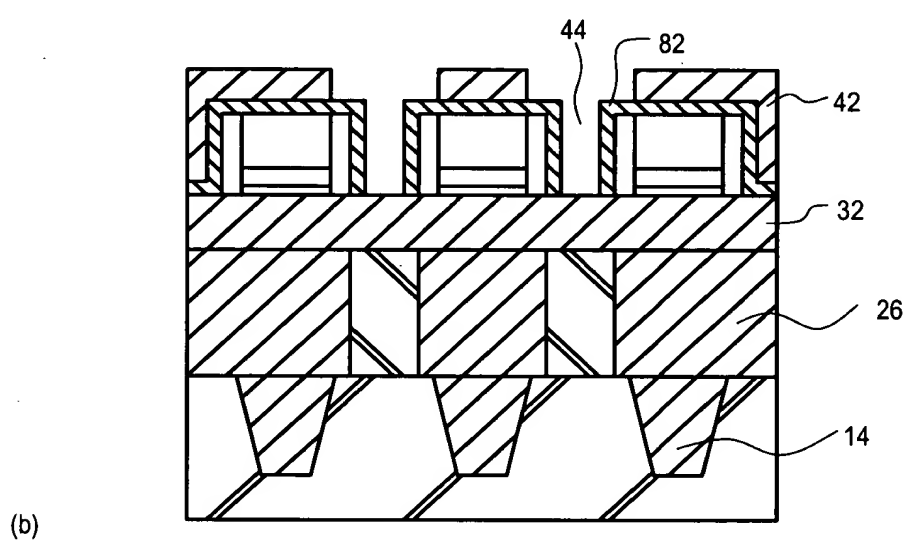
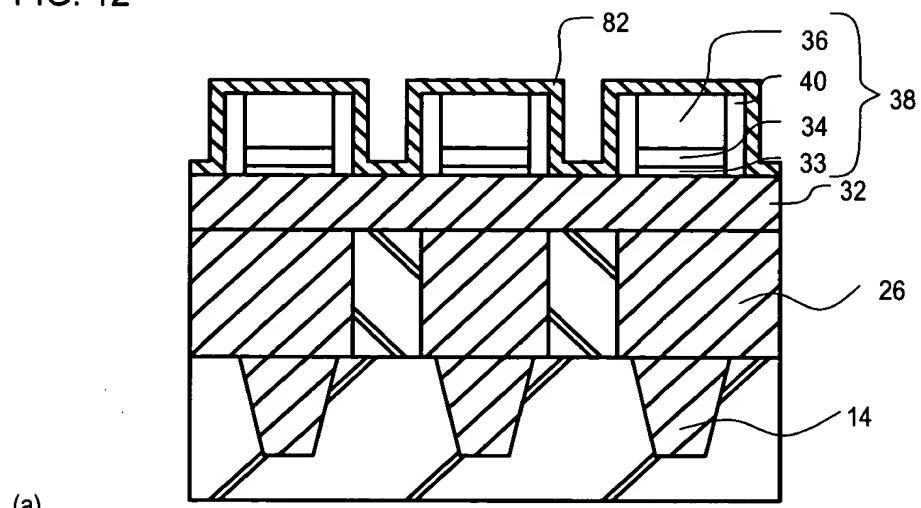
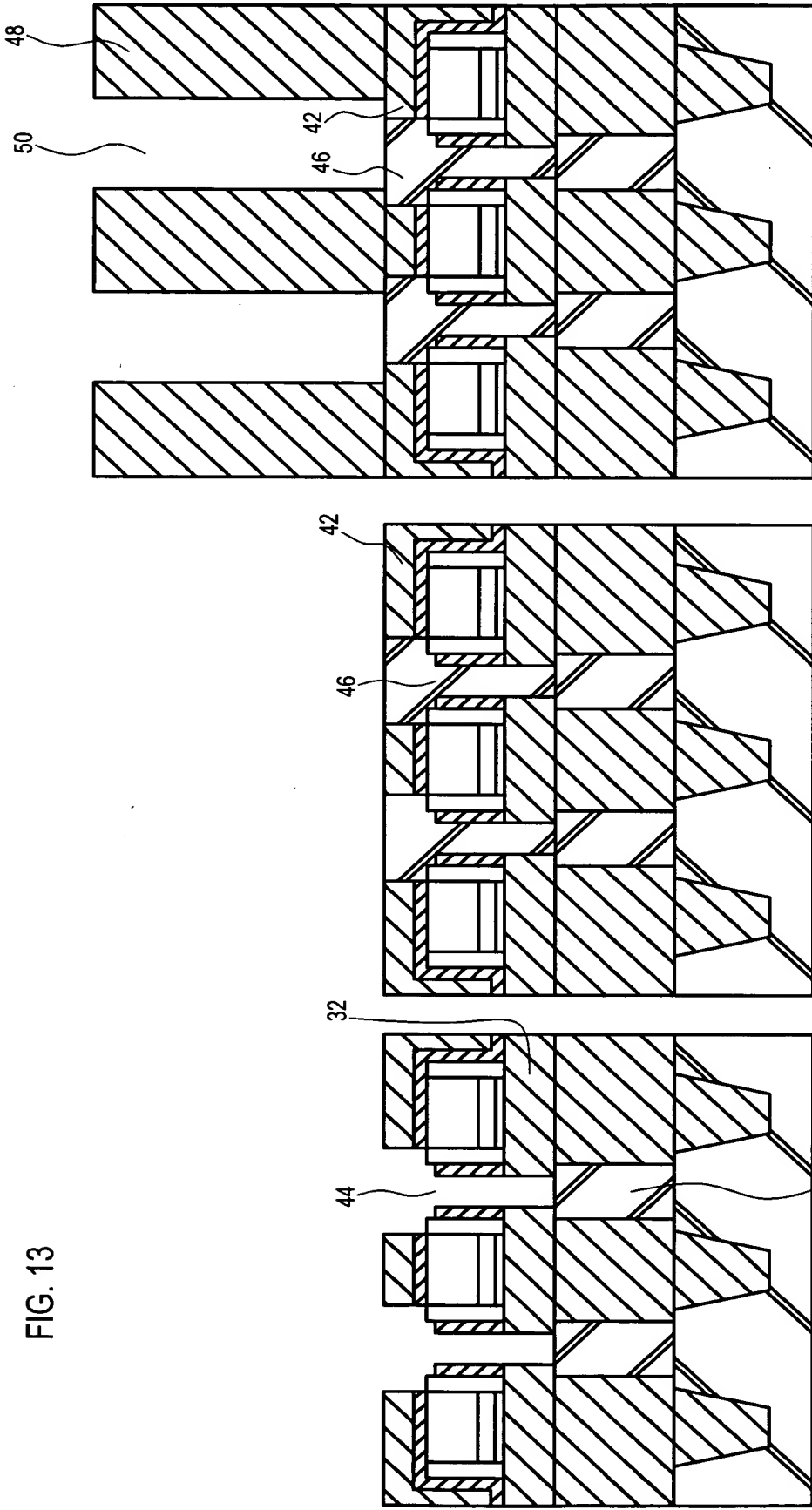


FIG. 12





(d)

(e)

(f)

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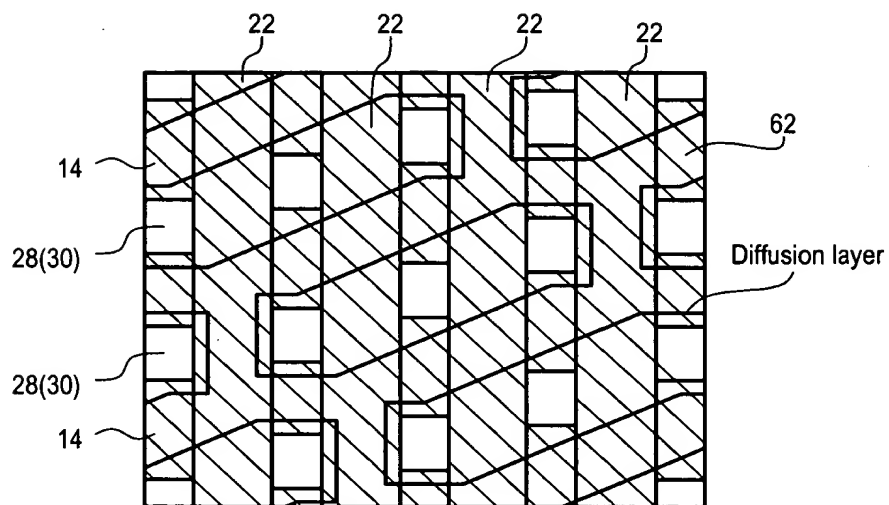


FIG. 14

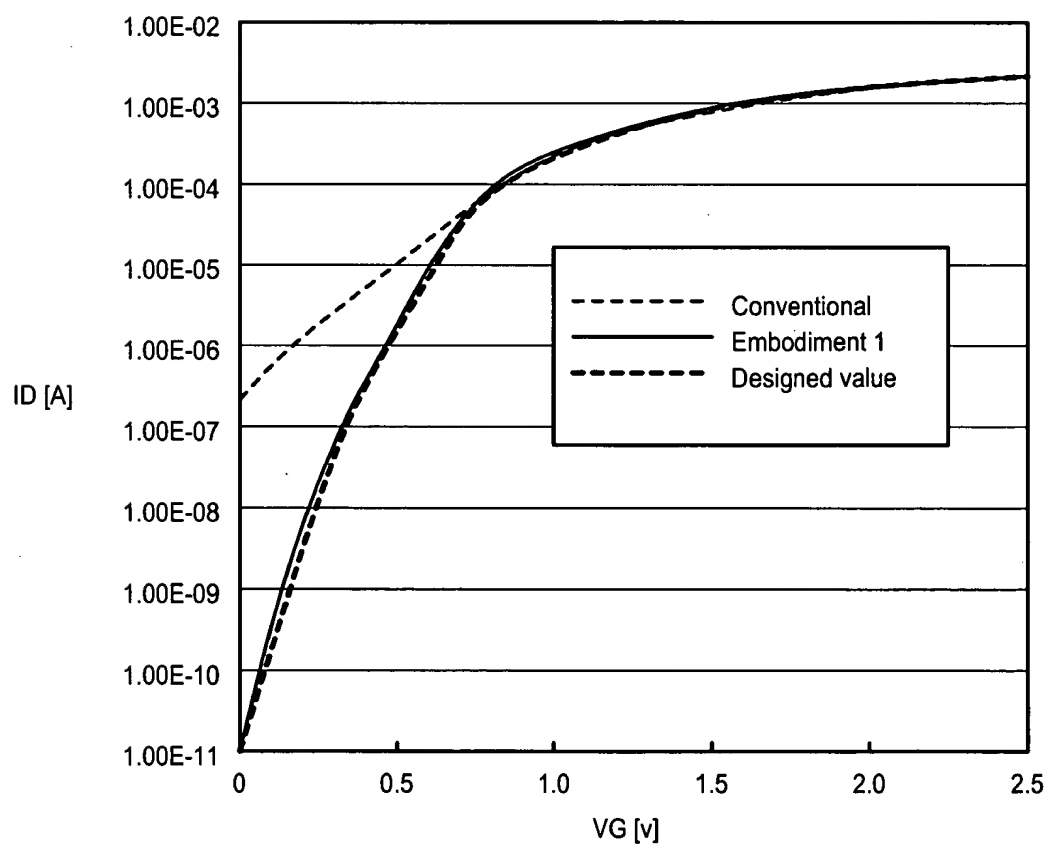


FIG. 15

Figure 10 consists of two cross-sectional views, (a) and (b), illustrating different configurations of a semiconductor device.

(a) This view shows a substrate 12 with a layer 14 on its top surface. A series of vertical structures are formed in the substrate, each containing a central core 26 surrounded by a shell 28. The cores are connected to a common horizontal line 30. The shells are connected to a common horizontal line 20. The entire assembly is covered by a protective layer 18. The bottom surface of the substrate is labeled 15. The top surface of the substrate is labeled 12. The label 10 points to the overall device structure.

(b) This view shows a similar substrate 12 with a layer 14 on its top surface. In this configuration, the vertical structures are formed directly in the substrate material, which is hatched to indicate it is solid. The cores 26 are connected to a common horizontal line 30. The shells 28 are also connected to a common horizontal line 30. The entire assembly is covered by a protective layer 18. The bottom surface of the substrate is labeled 15. The top surface of the substrate is labeled 12.

(b)

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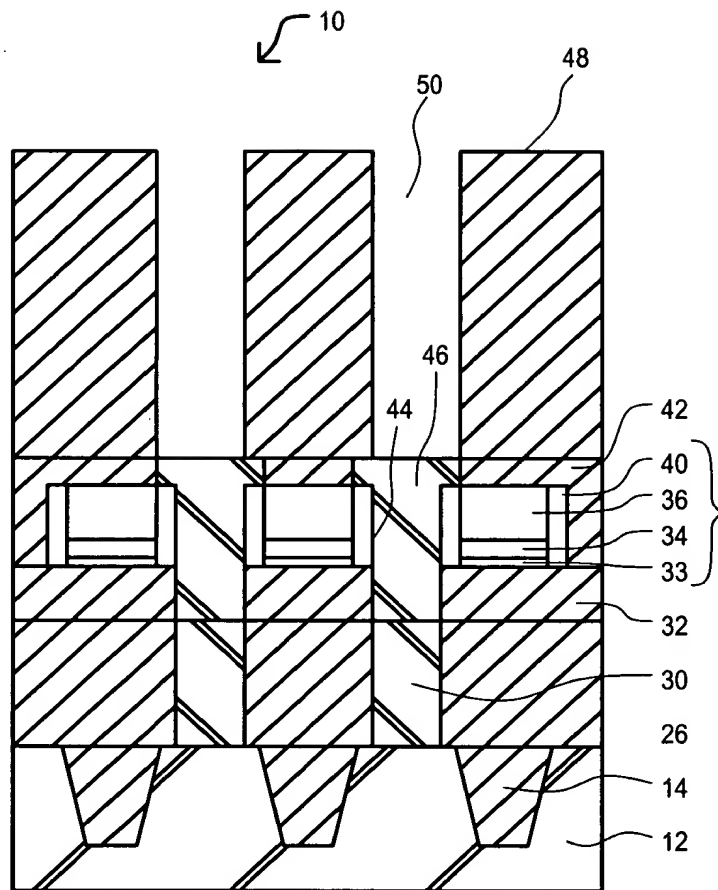
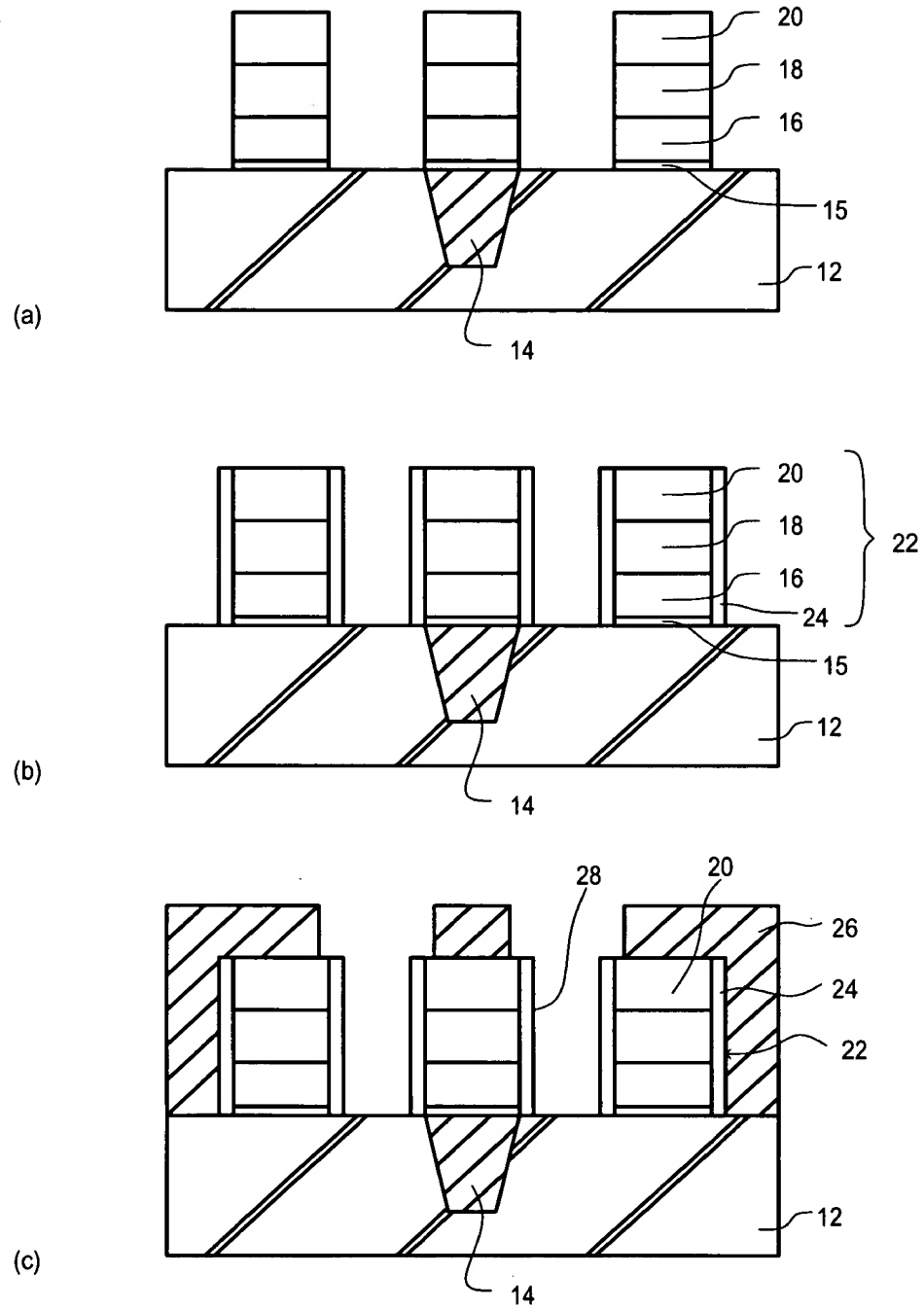


FIG. 17 (BACKGROUND ART)

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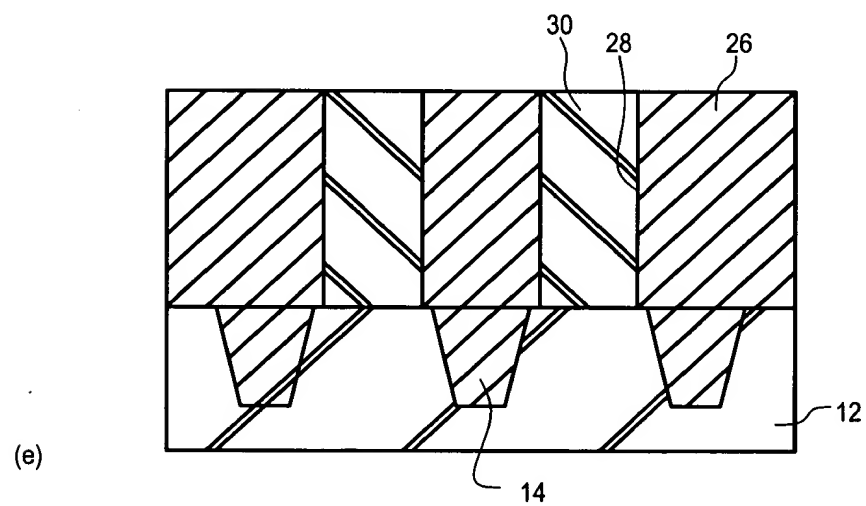
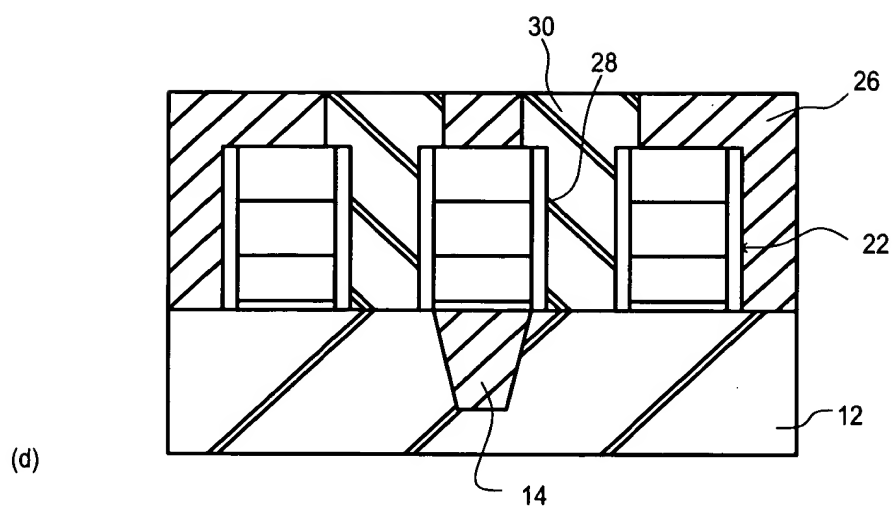


FIG. 19 (BACKGROUND ART)

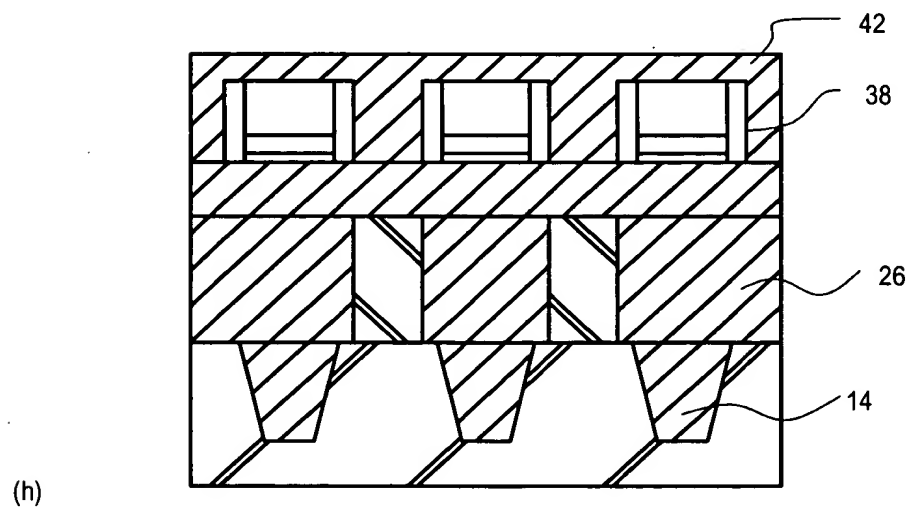
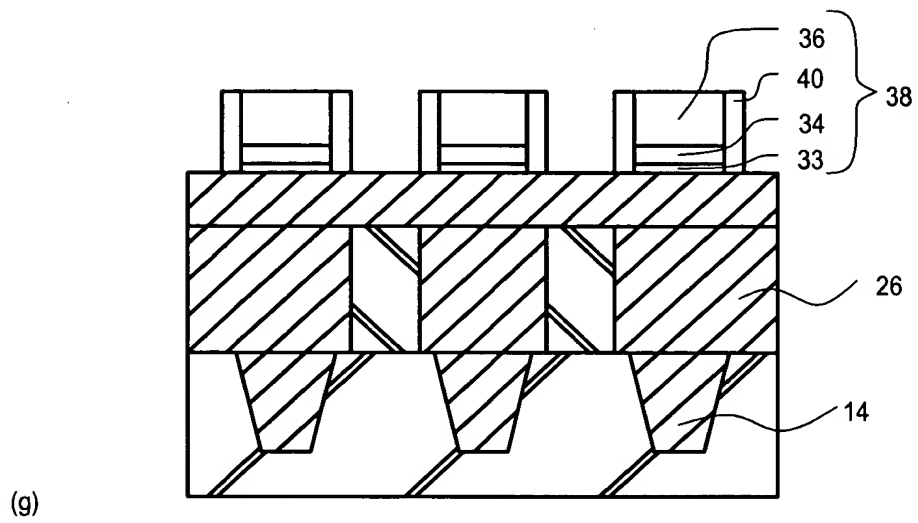
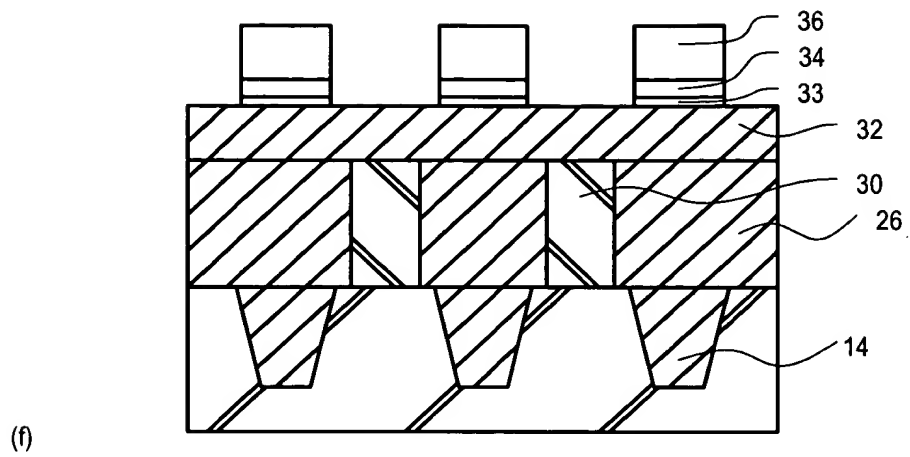


FIG. 20 (BACKGROUND ART)

